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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/127,584	07/31/98	RAYNAUD	A 02282.P055

LM02/0911
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EXAMINER	
SERGENT, D	
ART UNIT	**PAPER NUMBER**
2763	10

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/127,584	Applicant(s) RAYNAUD ET AL.	
	Examiner Douglas W. Sergent	Art Unit 2763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *06 June 2000* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 1998* is/are objected to by the Examiner.

11)☒ The proposed drawing correction filed on *06 June 2000* is: a)☒ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☐ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15)☒ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *9* .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other: .

DETAILED ACTION

1. Claims 1 – 33 are pending in this application. Claims 1, 5, 12, 16 and 20 have been amended, necessitating a new grounds of rejection. Claims 1 – 33 are rejected.

Response to Arguments

2. Applicant's arguments filed 6/6/00 have been fully considered but they are not persuasive. However, independent claims 1, 5, 12, 16 and 20 have been amended, therefore the examiner has produced a new grounds of rejection for these independent claims. The new rejections will be presented in the sections following. Arguments with respect to claims 24 – 33 are not deemed to be persuasive, therefore the previous rejections of these claims are maintained and are hereby incorporated by reference.

Drawings

3. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1–14, 16-18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al, and further in view of Kucukakar et al ("Matisse: An Architectural Design Tool for Commodity ICs) and Fang et al (A Real-Time RTL

Engineering-Change Method Supporting On-Line Debugging for Logic-Emulation Applications).

The current invention is generally directed to a debugging tool for use in circuit simulation. Specifically, the invention allows for statements to be inserted into synthesizable code (specifically RTL code) and then for the statements to be synthesized into netlist logic that functionally simulate debugging operations such as setting breakpoints and single step operation within a netlist description. This means that the breakpoint and single step functions would be available to the designer who is running a gate level simulation of the circuit.

With respect to claims 1 and 5, the claim indicates the identification of, or creation of a synthesizable statement (step a), followed by the actual synthesis of the code into a netlist instrumentation signal description (step b). This instrumentation signal defines a means for allowing observability and controllability (i.e. breakpoint) within the netlist code.

As indicated in the previous rejection Chen et al teaches a system (Matisse) for debugging 'synthesized' RTL designs (see Chen et al ABSRACT). The goal of Chen et al is, in part, to provide a methodology that is "analogous to source-level debugging of compiled software code, where the programmer debugs the execution of the compiled code while viewing the original source code" (pg. 134, col. 2, second paragraph). As Chen et al describes, this system generates RTL implementations from HLS designs (pg. 135, section 2.1). The applicant has argued that Chen et al teaches away from the synthesis of the code (pg. 137, section 3, second paragraph), however this does not

preclude that it could be done. Kucukakar et al further elaborates on the Matisse system which clearly states that Matisse is a debugger of the RTL implementation (pg. 29, Section ***Dynamic Execution Analysis***). In addition, Figure 7 in Kucukakar et al graphically shows all of the debugging features and the circuit to which they are applied.

Finally Fang et al shows a system where real-time changes in the RTL description of a circuit can be synthesized, maintaining established links between the RTL and netlist code (pg. 104, section 3.3). This means that changes in the RTL can quickly be debugged. It would have been obvious to one skilled in the art at the time of the applicant's invention to use the annotated design in Matisse in the Emulation in Fang et al, because this would allow the annotated design to be synthesized and produce the instrumentation signals of the current invention, thereby providing observability and controllability of the gate-level description.

With respect to Claim 2:

Chen et al teaches design annotation that includes embedding a daemon in the code describing a circuit element. This daemon is equivalent to the claimed instrumentation logic (pg. 137, sections 3, 3.1; pg. 138, section 3.2).

With respect to Claim 3 and 4:

Chen et al teaches execution analysis that allows for access to variables and operations of the design (pg. 138, section 4.1). The initialization of these variables and the updating of the variables (based on simulation results) is deemed to be inherent in the system of Chen et al.

With respect to Claim 6:

Chen et al teaches design annotation that includes embedding a daemon in the code describing a circuit element. The daemon performs the functions of inserting unique variable assignment statements for monitoring the output of the current circuit element (pg. 138, figure 3).

With respect to Claim 7:

Chen et al teaches execution analysis that allows for access to variables and operations of the design (pg. 138, section 4.1). The initialization of these variables and the updating of the variables (based on simulation results) is deemed to be inherent in the system of Chen et al.

With respect to Claim 8:

Chen et al teaches creation of instrumentation output signals for the sequential circuit operation (pg. 138, column 1, first paragraph).

With respect to Claim 9:

Chen et al generation cross-reference data mapping for the source code statements and the instrumented output signal (pg. 135, section 2.1).

With respect to Claim 10:

Chen et al teaches simulation of the design using instrumentation signals to establish simulation breakpoints (pg. 138, section 4.1).

With respect to Claim 11:

Chen et al teaches displaying the source code where the code execution is highlighted (pg. 138, section 4.1).

With respect to Claim 12, 16 and 20:

As described previously, Chen et al teaches a method and tools for manipulating a design description using High Level Synthesis (HLS) (as per claimed synthesizable statements). The design annotation process as described in Chen et al section 3 beginning on pg. 137 describes the process of inserting daemons into the source code that allow for the insertion of monitoring variables that can be monitored in the design process. Although Chen et al does not explicitly describe synthesizing the code into a gate-level design, this capability is inherent in the system as the system is used to produce a design description for manufacture.

Fang et al describes taking the modified RTL design and synthesizing this design (for implementation in an emulator). It would have been obvious to one skilled in the art at the time of the applicants invention to take the modified RTL code and produce a synthesized version of the circuit, as is shown in Fang, in order to either test the circuit design through simulation or emulation.

With respect to Claim 13, 17 and 22:

Chen et al teaches execution analysis that allows for access to variables and operations of the design (pg. 138, section 4.1). The initialization of these variables and the updating of the variables (based on simulation results) is deemed to be inherent in the system of Chen et al.

With respect to Claim 14, 18 and 23:

Chen et al teaches creation of instrumentation output signals for the sequential circuit operation (pg. 138, column 1, first paragraph). Chen et al teaches generation of

cross-reference data mapping for the source code statements and the instrumented output (pg. 135, section 2.1).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Postula et al teaches comparison of HLS and RTL designs.
- Orailoglu teaches synthesis of test circuitry that would be used for on-circuit testing (BIST).
- Howe teaches issues associated with simulation mismatches between RTL models and gatelevel models.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Sergent whose telephone number is (703)306-5448. The examiner can normally be reached on M-F (6:30 - 4:00) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703)305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-1396 for regular communications and (703)308-1396 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-5140.

Doug Sergent/DS
September 7, 2000

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER